IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yi Ding		
Assignee:	Mosel Vitelic, Inc.		
Title:	Fabrication Of Gate Dielectric In Nonvolatile Memories In Which A Memory Cell Has Multiple Floating Gates		
Application No.:	10/632,154	Filing Date:	July 30, 2003
Examiner:	Unknown	Group Art Unit:	Unassigned
Docket No.:	M-15230 US		

San Jose, California
April 16, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 CFR § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying form PTO-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;

2. a representation that a search has been made, other than as described above; or

3. an admission that the information cited herein is, or is considered to be material to patentability as defined in § 1.56(b).

No fee is believed to be required. If a fee is required for this Information Disclosure Statement, please charge the fee to Deposit Account No. 50-2257. This paper is being submitted in duplicate.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on April 16, 2004.

Michael Shenker 4-16-04
Attorney for Applicant Date of Signature

Respectfully submitted,

Michael Shenker

Michael Shenker
Attorney for Applicant(s)
Reg. No. 34,250

LAW OFFICES OF
MacPherson, Kwok, Chen & Heid LLP
1762 Technology Drive, Suite 226
San Jose, CA 95110
Telephone (408) 392-9520
Fax (408) 392-9262

U.S. Department of Commerce, Patent and Trademark Office	Atty Docket No.	Serial No.
	M-15230 US	10/632,154
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Applicant	
(Use several sheets if necessary)	Yi Ding	
	Filing Date	Group
	July 30, 2003	Unassigned

U.S. Patent Documents

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,420,231	16 Jul. 2002	Harari et al.			
	AB	2003/0218908 A1	27 Nov. 2003	Park et al.			
	AC	2004/0004863 A1	8 Jan. 2004	Wang			
	AD						
	AE						
	AF						
	AG						
	AH						

Foreign Patent Documents

							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AI	EP 0 938 098 A2	25 Aug. 1999	Europe				
	AJ							
	AK							
	AL							

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

	AM	United States Patent Application No. 10/798,475, entitled "Fabrication of Conductive Lines Interconnecting Conductive Gates in Nonvolatile Memories and Non-Volatile Memory Structures," Filed on March 10, 2004; Attorney Docket No. M-15296 US.
	AN	United States Patent Application No. 10/797,972, entitled "Fabrication of Conductive Lines Interconnecting First Conductive Gates in Nonvolatile Memories Having Second Conductive Gates Provided By Conductive Gates Lines, Wherein The Adjacent Conductive Gate Lines For The Adjacent Columns Are Spaced From Each Other, And Non-Volatile Memory Structures," Filed on March 10, 2004; Attorney Docket No. M-15297 US.
	AO	
	AP	

Examiner	Date Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.